REMARKS

Entry of the foregoing amendments after final rejection as narrowing the issues and presenting the claims in condition for allowance or better form for appeal is respectfully solicited. The foregoing amendments after final rejection have not been earlier presented because of the indicated allowable subject matter and the new grounds for rejection.

Claims 1-5, 7-15 and 16-20 are pending and at issue in the application with claims 1, 7, 14 and 16-18 being independent claims. Claims 1, 5, 8, 11, 14, 17 and 18 have been amended. Claim 6 has been canceled. Claims 7 and 16 have been allowed, and claims 3, 5, 6, 8-12 and 20 were indicated as allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Reconsideration and withdrawal of the rejections in view of the remarks below is respectfully requested.

The applicant respectfully traverses the rejection of claims 1, 2, 4 and 13 as anticipated by Lee (U.S. Patent No. 5,844,438). The Office action indicated that claim 5 would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Independent claim 1 has been amended to include all of the recitations of claim 5. Accordingly, the applicant respectfully submits that Lee does not disclose or suggest a circuit for generating an internal clock signal as recited in independent claim 1 or dependent claims 2-5 and 8-13.

The applicant respectfully traverses the rejections of claims 14, 18 and 19 as anticipated by Lee. Each of claims 14, 18 and 19 recite a circuit or method of generating an internal clock signal. The circuit or method outputs an external clock signal as an internal clock signal so that the internal clock signal has the same pulse width and same frequency as the external clock signal, if the external clock signal is a high frequency.

The applicant submits that claims 14, 18 and 19 are not anticipated or rendered obvious by Lee, because Lee does not teach each and every element of independent claims 14 and 18. In particular, the cited portions of Lee do not teach or suggest an apparatus or method that outputs an external clock signal as an internal clock signal having the same pulse

width and the same frequency as an external clock signal if the external clock signal is a high frequency, as recited in claims 14 and 18. Although Lee discloses a first internal clock generator 60 that generates a first internal clock (CLK1) as an internal clock (CLKDQ) when a system clock (CLK) is slow, and a second internal clock generator 70 that generates a second internal clock (CLK2) as the internal clock (CLKDQ) when the system clock (CLK is fast, the pulse width of the second internal clock (CLK2) is different from the pulse width of the system clock (CLK). Further, the phase of the second internal clock (CLK2) is different from the phase of the system clock (CLK), because the second internal clock (CLK2) is produced at the negative edge of the system clock (CLK). (Col. 9, ln. 52 to col. 10, ln. 25). As such, the internal clock generator 70 does not output an external clock signal as an internal clock signal so that the internal clock signal has the same pulse width and same frequency as the external clock signal, if the external clock signal is a high frequency.

The applicant further traverses the rejection of claim 17 as unpatentable over Lee. Claim 17 recites a method of generating an internal clock signal that includes generating a delayed external clock signal by delaying the external clock signal by some time, where the delayed external clock signal is used to generate an internal clock signal depending on whether the external clock signal is low frequency or high frequency. The external clock signal is generated as the external clock signal is low frequency, and the external clock signal is generated as the internal clock signal if the external clock signal is high frequency.

The applicant submits that claim 17 is not anticipated or rendered obvious by Lee, because Lee does not teach each and every element of the independent claim 1 and 4. In particular, the cited portions of Lee do not teach or suggest a method that generates a delayed external clock signal by delaying the external clock signal by some time, where the delayed external clock signal is used to generate an internal clock signal when the external clock signal is a low frequency, and where the external clock signal is used as the internal clock signal when the external clock signal is a high frequency. Lee discloses that when the system clock (CLK) is slow, a clock rate detector 50 produces a high output signal SS causing the internal clock (CLK1) to be generated for the internal clock (CLKDQ). (Column 10, lines 14-25). However, when the system clock (CLK) is fast, the clock rate detector (50) outputs a low level signal SS causing the internal clock (CLK2) to be generated for the internal clock

(CLKDQ). As a result, Lee does not disclose or suggest each and every element of independent claim 17.

Accordingly, the applicant respectfully submits that amended independent claims 1, 14, 17 and 18, and allowed independent claims 7 and 16 are novel and non-obvious in view of the cited references and should be allowed. Further dependent claims 2-5, 8-13, 19 and 20 which are dependent on the aforementioned independent claims are also submitted to be in allowable form. In light of the foregoing, the prompt issuance of a notice of allowance is respectfully solicited. Should the Examiner have any questions, the Examiner is respectfully invited to telephone the undersigned.

Respectfully submitted,

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